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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KNOLL, CLIFFORD H	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 06/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/904,085	HOUSE, RICHARD L.	
	Examiner	Art Unit	
	Clifford H Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to the communication filed 3/31/04. Currently claims 1-37 are pending.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

Claims 1-2, 4-10, 12-15, 17-22, 24-28, 30-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Liva (US 2002/0179720).

Regarding claim 1, Liva discloses first and second cards in a chassis with input and output nodes (e.g., paragraph [0019], "410", "415"); providing a facilitator card in the chassis having an input node connectable to the common bus and an output node connectable to an input node (e.g., paragraph [0019], "420"), connecting the input node of the second card to the output node of the redundancy facilitator card (e.g., paragraph [0019], "primary I/O card 420 re-routes RF traffic..."), connecting the input node of the first card, thereby coupling the input node of the first card to the input node of the second card to provide redundancy (e.g., paragraph [0023]).

Regarding claim 2, Liva also discloses connecting the input node of the second card to the output node of the facilitator card by a cable (e.g., paragraph [0019], "The interconnects between additional I/O card 425...").

Regarding claim 4, Liva also discloses connecting the input node to the output node of the first card after determining a failure has occurred (e.g., paragraph [0022]).

Regarding claim 5, Liva also discloses a line card (e.g., paragraph [0019]).

Regarding claim 6, Liva also discloses a network interface card as the first card (e.g., paragraph [0003]).

Regarding claim 7, Liva also discloses connecting the input node of the second card to the output node of the redundancy facilitator card by a cable and a pair of interface connectors disposed on a backplane (e.g., paragraph [0019]).

Regarding claim 8, Liva also discloses circuitry to perform a function and a switch to connect the input node of the card to either the output node or the circuitry of the card (e.g., paragraph [0022]).

Regarding claim 9, Liva also discloses connecting the input node of the second card to a first interface connector located on a backplane of the chassis and connecting the output node of the facilitator card to a second interface connector located on the backplane (e.g., paragraph [0019], Figure 5).

Regarding claim 10, Liva also discloses connecting the first interface connector to the second interface connector by a cable (e.g., paragraph [0019]).

Regarding claim 12, Liva also discloses connecting the first connector to the second interface connector by conductors formed on the backplane (e.g., paragraph [0019]).

Regarding claim 13, Liva also discloses a portion of the common bus is formed on the backplane of the chassis.

Regarding claim 14, Liva discloses first and second cards in a chassis (e.g., paragraph [0019], "410", "415"), providing a test card (e.g., paragraph [0025]), connecting the input node of the second card to the output node of the test card (e.g., Figure 5), connecting the input node of the first card to the associated output node of the first card and connecting the input node of the test card to the test circuitry (e.g., paragraph [0019]).

Regarding claim 15, Liva also discloses connecting the input node of the second card to the output node of the test card by a cable (e.g., paragraph [0019]).

Regarding claim 17, Liva also discloses a line card (e.g., paragraph [0019]).

Regarding claim 18, Liva also discloses a network interface card as the first card (e.g., paragraph [0003]).

Regarding claim 19, Liva also discloses connecting the input node of the second card to the output node of the test card by a cable and a pair of interface connectors, the interface connectors disposed on a backplane of the chassis (e.g., paragraph [0019]).

Regarding claim 20, Liva also discloses circuitry to perform a function and a switch to connect the input node of the card to either the output node or the circuitry of the card (e.g., paragraph [0022]).

Regarding claim 21, Liva also discloses connecting the input node of the second card to the output node of the test card by a cable and a pair of interface connectors disposed on a backplane and connecting the output node of the test card to a second interface connector located on the backplane (e.g., paragraph [0019]).

Regarding claim 22, Liva also discloses connecting the first interface connector to the second interface connector by a cable (e.g., paragraph [0019]).

Regarding claim 24, Liva also discloses connecting the first interface connector to the second interface connector by conductors formed on the backplane (e.g., paragraph [0019]).

Regarding claim 25, Liva also discloses the common bus portion formed on a backplane (e.g., paragraph [0019]).

Regarding claim 26, Liva also discloses a chassis, first and second cards with logic, input and output nodes (e.g., paragraph [0019]), a switch operable to connect the input node of the card to either the output node of the card or the card logic (e.g., Figure 5), a facilitator card disposed in one of the slots having input and output nodes and a first connector operable to connect the input node to the output node (e.g., paragraph [0019], "420"), where the backplane comprises a bus connected to the output nodes of the cards and the input node of the facilitator card and a second connector connecting the output node of the facilitator card to the input node of the second card (e.g., Figure 5).

Regarding claim 27, Liva also discloses the second connector comprises a cable (e.g., paragraph [0019]).

Regarding claim 28, Liva also discloses the pair of interface connectors (e.g., paragraph [0019]).

Regarding claim 30, Liva also discloses the switch (e.g., Figure 5).

Regarding claim 31, Liva also discloses a conductor connecting the input node of the facilitator card to the output node of the facilitator card (e.g., Figure 5).

Regarding claim 32, Liva also discloses the test circuitry and a switch further operable to selectively connect the input node of the3 facilitator card to the test circuitry (e.g., paragraph [0022]).

Regarding claim 33, Liva also discloses a line card (e.g., paragraph [0019]).

Regarding claim 34, Liva also discloses a network interface card as the first card (e.g., paragraph [0003]).

Regarding claim 35, Liva discloses first and second cards, and means for selectively connecting the input node of the first card to the output node of the first card and means for connecting the output node of the first card to the input node of the second card (e.g., Figure 5).

Regarding claim 36, Liva also discloses a line card (e.g., paragraph [0019]).

Regarding claim 37, Liva also discloses a network interface card as the first card (e.g., paragraph [0003]).

Claim Rejections - 35 USC § 103

Claims 3, 11, 16, 23, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liva as applied above, further in view of Heilmann (US 2003/0112940).

Regarding claims 3, 11, 16, 23, and 29, Liva also discloses the use of a multi-pin pair cable, but does not expressly mention the particular implementation of a twenty-five pair cable; however Heilmann discloses this detail (e.g., paragraph [0042]). It would have been obvious to combine Heilmann with Liva because Heilmann teaches the advantages of using a conventional cable arrangement (e.g., paragraph [0028]) in implementing the multi-pin pair cable of Liva. Therefore, it would be obvious to one of ordinary skill in the art to combine Heilmann with Liva at the time the invention was made.

Response to Arguments

Applicant's arguments filed 3/31/04 have been fully considered but they are not persuasive.

Applicant argues that "[t]he provisional application discloses neither the material relied on in rejecting the claims, nor each and every limitation of the claims, and for this reason alone, the rejections of the claims based on the '720 Publication are improper. In particular, the Office Action relies on the embodiments of Figures 4 and 5 of the '720 Publication, yet neither these figures nor any equivalent figures or designs are provided in the provisional application" (p. 11); however this is incorrect. The provisional application provides the appropriate figures and supporting disclosure; in particular, the third figure in the Appendix, with lead-in "[a] set of line cards can be connected like this", is illustrative of the enabling disclosure of the provisional application.

Applicant further argues that the claim 1 recitation of "coupling the input node of the first card to the input node of the second card to provide redundancy for the first card by connecting the input node of the first card to the associated output node of the first card"; and in particular, notes the failure to disclose "connecting the input node of the first card to the associated output node of the first card" (p. 12); however these features are in fact disclosed by the prior art. For example, in the provisional application, the figure from the Appendix, referred to supra , shows a "Line Card #1" with a clear depiction of a switch (the lower switch) which connects the input ("RF In") and output node ("B/U Bus In") of the first card. This does provide the redundancy claimed, where it can be seen disclosed on the same page as the figure, "[i]f any line card fails, its RF switches can be thrown, which will disconnect its signals from the rear connectors, and steer the inputs and outputs of the 'Designated Backup' to them instead"; thus the prior art adequately discloses the "coupling" as to "provide redundancy".

Applicant further argues that as distinct from the claimed invention, Liva discloses "coupling of these nodes to other connections – but not to each other" (p. 12); however, as described regarding the provisional application supra, when the switches are "thrown" as disclosed, the input of "Line Card #1" is connected to the input of the "Declared Backup" (Figure), which constitutes connecting nodes to each other.

Thus Examiner maintains the rejection of claim 1 using Liva. As Applicant raises the issue of inadequate disclosure in the provisional Application, Examiner has based

his response on disclosure from the provisional Application; the parallels to the publication relied upon and cited in the rejection maintained above are clear.

Applicant argues that in claim 26, the publication "does not show 'a switch [on the first and second cards operable to selectively connect the input node of the card to either the output node of the card or the card logic'" (p. 12); however, the switch of the provisional application referred to supra achieves just these functions as expounded supra. Applicant further argues that the coupling of connections refer to "other connections – but not to each other" (p. 12); however, as expounded regarding claim 1 supra, the coupling occurs between the recited nodes.

Thus the rejections using Liva are maintained.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Madonna (US 5596569) discloses switched redundant line cards (e.g., col. 8, lines 25-48); Deschaine (US 5901024) is similarly pertinent (e.g., col. 4, lines 15-23).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 703-305-8656. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

chk

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